CLAIMS

What is claimed is:

1. A system comprising:
a radio frequency integrated circuit including
a single bit modulator to convert an analog signal into a serial digital bit stream, and
an output driver coupled to the single bit sigma delta modulator, the output driver to drive the serial digital bit stream out from the radio frequency integrated circuit;
and
a digital signal processing integrated circuit including
an input receiver coupled to the output driver of the radio frequency integrated circuit, the input receiver to receive the serial digital bit stream, and
a decimator coupled to the input receiver, the decimator to receive the serial digital bit stream, lower a sampling rate of the serial digital bit stream and convert the serial digital bit stream into parallel digital data samples.

2. The system of claim 1, wherein
the digital signal processing integrated circuit further includes
a demodulator to digitally demodulate the parallel digital data samples into data words for

further signal processing by the digital signal processing integrated circuit.

3. The system of claim 1, wherein the single bit modulator is a single bit sigma delta modulator.

4. The system of claim 1, wherein the single bit modulator is a single bit delta modulator.

5. The system of claim 1, wherein the single bit modulator is a single bit analog to digital converter and a modulator coupled together.

6. The system of claim 1, wherein the output driver has a low voltage output swing, the output driver to drive the serial digital bit stream out of the radio frequency integrated circuit with the low voltage output swing.

7. The system of claim 6, wherein the input receiver to receive the serial digital bit stream with the low voltage output swing.

8. The system of claim 7, wherein the input receiver further to increase the low voltage output swing of the serial digital bit stream within the digital signal processing integrated circuit.

9. The system of claim 6, wherein

the low voltage output swing between a high logic level and a low logic level is less than an output swing between a high logic level and a low logic level of a three volt complementary metal oxide semiconductor (CMOS) process technology.

10. The system of claim 6, wherein

the low voltage output swing between a high logic level and a low logic level is less than an output swing between a high logic level of 1.8 volts and a low logic level of 0.2 volts.

11. The system of claim 8, wherein

the output driver translates first voltage levels of a first output voltage swing of the serial digital bit stream into second voltage levels with a second output voltage swing less than the first output voltage swing, and

the input receiver translates the second voltage levels of the second output voltage swing into third voltage levels with a third output voltage swing greater than the second output voltage swing.

12. The system of claim 11, wherein

the third voltage levels are substantially the same as the first voltage levels.

13. The system of claim 1, wherein

the output driver is double ended and generates a differential signal to represent the serial digital bit stream, and

the input receiver has a differential input to receive the differential signal to represent the serial digital bit stream.

14. The system of claim 13, wherein

the output driver is a low voltage differential signaling transmitter to generate a low voltage differential output signal with a low voltage differential swing, and

the input receiver is a low voltage differential signaling receiver to receive the low voltage differential output signal with the low voltage differential swing.

15. The system of claim 14, wherein

the low voltage differential swing is at least 100 milli-volts.

16. The system of claim 1, wherein

the serial digital bit stream is a rectangular waveform.

17. The system of claim 1, wherein

the radio frequency integrated circuit is a receiver.

18. The system of claim 1, wherein

the radio frequency integrated circuit is a transceiver.

19. The system of claim 1, wherein

a delta sigma clock is coupled to the single bit sigma delta modulator, a frequency of the delta sigma clock to provide a data rate in the serial digital bit stream.

20. The system of claim 19, wherein

the frequency of the delta sigma clock is programmable to provide various data rates in the serial digital bit stream for various wireless communication systems.

21. The system of claim 1, wherein

a low frequency reference clock couples between the radio frequency integrated circuit and the digital signal processing integrated circuit to synchronize clock signals of each.

22. The system of claim 21, wherein

the low frequency reference clock synchronizes a sigma delta clock of the radio frequency integrated circuit with a local clock of the digital signal processing integrated circuit.

23. A radio frequency integrated circuit comprising:

at least one gain amplifier to couple to an antenna to receive a first wireless radio frequency signal of a first selectable carrier frequency;

at least one down converter coupled to the at least one gain amplifier, the at least one down converter to extract a first analog signal from the first wireless radio frequency signal;

at least one single bit sigma delta modulator coupled to the at least one down converter, the at least one single bit sigma delta modulator to convert the first analog signal into a first serial digital bit stream; and

at least one output driver coupled to the at least one single bit sigma delta modulator, the at least one output driver to provide a low voltage output swing of the first serial digital bit stream to reduce noise generation as the first serial digital bit stream is coupled to another integrated circuit.

24. The radio frequency integrated circuit of claim 23, further comprising

a second gain amplifier to couple to the antenna to simultaneously receive a third wireless radio frequency signal of a third selectable carrier frequency;

a second down converter coupled to the second gain amplifier, the second down converter to extract a third analog signal from the third wireless radio frequency signal;

a second single bit sigma delta modulator coupled to the second down converter, the second single bit sigma delta modulator to convert the third analog signal into a third serial digital bit stream; and

a second output driver coupled to the second single bit sigma delta modulator, the second output driver to provide a low voltage output swing of the third serial digital bit stream to reduce noise

generation as the third serial digital bit stream is coupled to another integrated circuit.

25. The radio frequency integrated circuit of claim 23, wherein

the at least one gain amplifier is a variable gain amplifier or a switched gain amplifier.

26. The radio frequency integrated circuit of claim 24, wherein

the at least one gain amplifier and the second gain amplifier are variable gain amplifiers or switched gain amplifiers.

27. The radio frequency integrated circuit of claim 23, wherein

the radio frequency integrated circuit is a radio frequency receiver integrated circuit.

28. The radio frequency integrated circuit of claim 23, wherein

the radio frequency integrated circuit is a transceiver and further includes,

an input receiver to receive a second serial digital bit stream to be transmitted;

a data recoverer coupled to the input receiver, the data recoverer to recover digital data bits from the second serial digital bit stream;

a low pass filter coupled to the data recoverer, the low pass filter to convert the digital data bits into a second analog signal;

a mixer coupled to the low pass filter, the mixer to up-convert the second analog signal from a baseband frequency to a second selectable carrier frequency as a second wireless radio frequency signal; and

an amplifier coupled to the mixer, the amplifier to amplify the second wireless radio frequency signal for broadcast over the antenna.

29. The radio frequency integrated circuit of claim 28, wherein

the first selected carrier frequency and the second selected carrier frequency are selected from a set of carrier frequencies of a first selected wireless communication system.

30. The radio frequency integrated circuit of claim 29, wherein

the selected wireless communication system is selected from the set of Universal Mobile Telecommunication System (UMTS), Global System for Multiple Communication (GSM), GSM Mobile Application Part (GSM-MAP), General Packet Radio Protocol System or General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), (GAIT), Orthogonal Frequency-Division Multiplexing (OFDM), Code Orthogonal Frequency Division Multiplexing (COFDM), Block Coding, Convolutional Coding, Turbo Coding, Trellis Coding,

Gaussian Minimum Shift Keying (GMSK), Quadrature Phase Shift Keying (QPSK), Quadrature Amplitude Modulation (QAM), Frequency Modulation (FM), Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA), Code Division Multiple Access (CDMA), Narrowband CDMA (N-CDMA), Wideband CDMA (W-CDMA), CDMA2000, CDMA2000-1XEV, CDMA2000-EVDO, CDMA2000-EDV, Time Division-Synchronized Code Division Multiple Access (TD-SCDMA), Third-Generation Partnership Project (3GPP TDD), International Mobile Telecommunication (IMT), IMT2000MC, IMT2000DS, IMT2000SC, IMT2000TC, Personal Communication System (PCS), Digital Communication System (DCS), Personal Digital Cellular (PDC), Digital Enhanced Cordless Telecommunications (DECT), Advanced Mobile Phone System (AMPS), Wireless Local Area Network (LAN) (IEEE 802.11a, IEEE 802.11b, IEEE 802.11g), and Global Positioning System (GPS).

31. The radio frequency integrated circuit of claim 29, wherein

the first selected carrier frequency is selected from a set of carrier frequencies of a Universal Mobile Telecommunication System (UMTS), Global System for Multiple Communication (GSM), GSM Mobile Application Part (GSM-MAP), General Packet Radio Protocol System or General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), (GAIT), Orthogonal Frequency-Division Multiplexing (OFDM), Code Orthogonal Frequency Division Multiplexing (COFDM), Gaussian Minimum Shift Keying (GMSK), Quadrature Phase Shift Keying (QPSK), Quadrature Amplitude Modulation (QAM), Frequency

Modulation (FM), Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA), Code Division Multiple Access (CDMA), Narrowband CDMA (N-CDMA), Wideband CDMA (W-CDMA), CDMA2000, CDMA2000-1XEV, CDMA2000-EVDO, CDMA2000-EDV, Time Division-Synchronized Code Division Multiple Access (TD-SCDMA), Third-Generation Partnership Project (3GPP TDD), International Mobile Telecommunication (IMT), IMT2000MC, IMT2000DS, IMT2000SC, IMT2000TC, Personal Communication System (PCS), Digital Communication System (DCS), Personal Digital Cellular (PDC), Digital Enhanced Cordless Telecommunications (DECT), Advanced Mobile Phone System (AMPS), Wireless Local Area Network (LAN) (IEEE 802.11a, IEEE 802.11b, IEEE 802.11g), and Global Positioning System (GPS), and

the second selected carrier frequency is selected from a set of carrier frequencies of Universal Mobile Telecommunication System (UMTS), Global System for Multiple Communication (GSM), GSM Mobile Application Part (GSM-MAP), General Packet Radio Protocol System or General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), (GAIT), Orthogonal Frequency-Division Multiplexing (OFDM), Code Orthogonal Frequency Division Multiplexing (COFDM), Gaussian Minimum Shift Keying (GMSK), Quadrature Phase Shift Keying (QPSK), Quadrature Amplitude Modulation (QAM), Frequency Modulation (FM), Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA), Code Division Multiple Access (CDMA), Narrowband CDMA (N-CDMA), Wideband CDMA (W-CDMA), CDMA2000, CDMA2000-1XEV, CDMA2000-EVDO, CDMA2000-EDV, Time Division-Synchronized

Code Division Multiple Access (TD-SCDMA), Third-Generation Partnership Project (3GPP TDD), International Mobile Telecommunication (IMT), IMT2000MC, IMT2000DS, IMT2000SC, IMT2000TC, Personal Communication System (PCS), Digital Communication System (DCS), Personal Digital Cellular (PDC), Digital Enhanced Cordless Telecommunications (DECT), Advanced Mobile Phone System (AMPS), and Wireless Local Area Network (LAN) (IEEE 802.11a, IEEE 802.11b, IEEE 802.11g).

32. A radio frequency integrated circuit comprising:

an input receiver to receive a serial digital transmission bit stream with a reduced output voltage swing, the input receiver to increase the output voltage swing of the serial digital transmission bit stream in the radio frequency integrated circuit;

a data recoverer coupled to the input receiver, the data recoverer to recover digital data bits from the serial digital transmission bit stream;

a low pass filter coupled to the data recoverer, the low pass filter to convert the digital data bits into an analog transmission signal;

a mixer coupled to the low pass filter, the mixer to up-convert the analog transmission signal from a baseband frequency to a selectable carrier frequency as a transmit radio frequency signal; and

an amplifier coupled to the mixer, the amplifier to amplify the transmit radio frequency signal for broadcast over an antenna.

33. The radio frequency integrated circuit of claim 32, wherein

the radio frequency integrated circuit is a transmitter.

34. A method for a wireless radio, the method comprising:

receiving a first wireless radio signal;

extracting a first analog signal from the first wireless radio signal;

converting the first analog signal into a first serial digital data signal;

providing a low voltage output swing in the first serial digital data signal; and

transmitting the first serial digital data signal with the low voltage output swing from a radio frequency (RF) integrated circuit to a digital signal processing (DSP) integrated circuit.

35. The method of claim 34, further comprising:

receiving a second wireless radio signal;

extracting a second analog signal from the second wireless radio signal;

converting the second analog signal into a second serial digital data signal;

providing a low voltage output swing in the second serial digital data signal; and

transmitting the second serial digital data signal with the reduced output voltage swing from the radio frequency integrated circuit to the digital signal processing (DSP) integrated circuit.

36. The method of claim 35, wherein
the first wireless radio signal and the second wireless radio signal are simultaneously received.

37. The method of claim 35, wherein
the first analog signal and the second analog signal are simultaneously extracted.

38. The method of claim 35, wherein
the first wireless radio signal is received during the time period that the second wireless radio signal is received.

39. The method of claim 35, wherein
the first analog signal is extracted during the time period that the second analog signal is extracted.

40. The method of claim 35, further comprising:
receiving a third wireless radio signal;
extracting a third analog signal from the third wireless radio signal;
converting the third analog signal into a third serial digital data signal;
providing a low voltage output swing in the third serial digital data signal; and
transmitting the third serial digital data signal with the low output voltage swing from a radio integrated circuit to a digital signal processing (DSP) integrated circuit.

41. The method of claim 40, wherein
the first wireless radio signal, the second wireless radio signal, and the third wireless radio signal are simultaneously received.

42. The method of claim 41, wherein
the first analog signal, the second analog signal, and the third analog signal are simultaneously extracted.

43. The method of claim 34, further comprising:
receiving the first serial digital data signal with the reduced output voltage swing;
increasing the output voltage swing in the first serial digital data signal;
reducing a sampling frequency of the first serial digital data signal; and
converting the first serial digital data signal into a parallel digital data signal for processing by the DSP integrated circuit.

44. The method of claim 34, wherein
the converting of the first analog signal into the first serial digital data signal is a delta-sigma modulation of the first analog signal into the first serial digital data signal.

45. The method of claim 43, further comprising:

recovering data words from the parallel digital data signal by digital demodulation for a predetermined wireless communication system.

46. The method of claim 34, wherein
the transmitting of the first serial digital data signal is over a single wire.

47. The method of claim 34, wherein
the first serial digital data signal is a differential data signal, and
the transmitting of the first serial digital data signal is over a pair of wires.

48. The method of claim 34, wherein
the first serial digital data signal is a complex differential data signal and the transmitting of the first serial digital data signal is over two pairs of wires,
a first differential data signal of the first serial digital data signal is transmitted over the first pair of wires, and
a second differential data signal of the first serial digital data signal is transmitted over the second pair of wires.

49. The method of claim 48, wherein
the first differential data signal is a real component of a complex data signal, and
the second differential data signal is an imaginary component of the complex data signal.

50. The method of claim 48, wherein
the first differential data signal is an in-phase signal, and
the second differential data signal is a quadrature signal with respect to the in-phase signal.

51. The method of claim 34, wherein
the first serial digital data signal is a multiphase differential data signal and the transmitting of the first serial digital data signal is over two pairs of wires,
a magnitude data signal of the first serial digital data signal is transmitted over the first pair of wires, and
a phase data signal of the first serial digital data signal is transmitted over the second pair of wires.

52. The method of claim 34, further comprising:
receiving a fourth serial digital data signal from the DSP integrated circuit for transmission over a wireless communication system;
converting the fourth serial digital data signal from the DSP integrated circuit into a fourth analog signal;
up-converting the fourth analog signal to a selectable carrier frequency; and
transmitting the fourth analog signal through the antenna as a fourth wireless radio frequency signal.

53. The method of claim 52, wherein

the fourth serial digital data signal from the DSP integrated circuit is a low voltage output swing signal, and the method further includes

increasing the low voltage output swing in the fourth serial digital data signal from the DSP integrated circuit.

54. A data signal flow between a radio frequency integrated circuit and a digital signal processing (DSP) integrated circuit, the data signal flow comprising:

a first serial digital data signal flowing from the radio frequency integrated circuit to the DSP integrated circuit, the first serial digital data signal representing a first received data signal from a first wireless communication system; and

a second serial digital data signal flowing from the radio frequency integrated circuit to the DSP integrated circuit, the second serial digital data signal representing a second received data signal from a second wireless communication system.

55. The data signal flow of claim 54, wherein

the first serial digital data signal is a complex differential data signal flowing over two pairs of wires,

an in-phase differential data signal of the first serial digital data signal flows over a first pair of wires, and

a quadrature differential data signal with respect to the in-phase differential data signal of the first serial digital data signal flows over a second pair of wires.

56. The data signal flow of claim 54, wherein

the first serial digital data signal is a multiphase differential data signal flowing over two pairs of wires,

a magnitude data signal of the first serial digital data signal flows over a first pair of wires, and

a phase data signal of the first serial digital data signal flows over a second pair of wires.

57. The data signal flow of claim 54, further comprising:

a third serial digital data signal flowing from the DSP integrated circuit to the radio frequency integrated circuit, the third serial digital data signal representing a first transmit data signal for communication over the first wireless communication system.

58. The data signal flow of claim 57, wherein

the third serial digital data signal is a complex differential data signal flowing over two pairs of wires,

an in-phase differential data signal of the third serial digital data signal flows over a first pair of wires, and

a quadrature differential data signal with respect to the in-phase differential data signal of the third serial digital data signal flows over a second pair of wires.

59. The data signal flow of claim 57, wherein

the third serial digital data signal is a multiphase differential data signal flowing over two pairs of wires,

a magnitude data signal of the third serial digital data signal flows over a first pair of wires, and

a phase data signal of the third serial digital data signal flows over a second pair of wires.

60. The data signal flow of claim 54, wherein

the first serial digital data signal is a low voltage differential data signal flowing over at least one pair of wires.

61. The data signal flow of claim 57, wherein

the third serial digital data signal is a low voltage differential data signal flowing over at least one pair of wires.

62. The data signal flow of claim 54, wherein

a data rate of the first serial digital data signal is variable to adapt to a selected wireless communication system.

63. The data signal flow of claim 57, wherein

a data rate of the first serial digital data signal, a data rate of the second serial digital data signal, and a data rate of the third serial digital data signal are variable to adapt to selected wireless communication systems.

64. The data signal flow of claim 54, wherein

the first serial digital data signal and the second serial digital data signal simultaneously flow from the radio frequency integrated circuit to the DSP integrated circuit to simultaneously receive data over two wireless channels of communication.

65. The data signal flow of claim 57, wherein

the first serial digital data signal, the second serial digital data signal, and the third serial digital data signal simultaneously flow between the radio frequency integrated circuit and the DSP integrated circuit to

simultaneously receive data over two wireless channels of communication and

simultaneously transmit data over one wireless channel of communication.

66. A radio frequency integrated circuit comprising:

a plurality of gain amplifiers to couple to an antenna to simultaneously receive wireless radio frequency signals of selectable carrier frequencies;

a plurality of down converters coupled to the plurality of gain amplifiers, the plurality of down converters to simultaneously extract analog signals from the wireless radio frequency signals; and

a plurality of sigma delta modulators coupled to the plurality of down converters, the plurality of single bit sigma delta modulators to simultaneously convert the analog signals into serial digital bit streams; and

a plurality of output drivers coupled to the plurality of single bit sigma delta modulators, the plurality of output drivers to couple the serial digital bit streams to another integrated circuit.

67. The radio frequency integrated circuit of claim 66, wherein,

the plurality of output drivers further to reduce an output voltage swing of the serial digital bit streams to further reduce noise generation as the serial digital bit streams are coupled to the another integrated circuit.

68. The radio frequency integrated circuit of claim 66, wherein

the plurality of gain amplifiers are a variable gain amplifier or a switched gain amplifier.

69. The radio frequency integrated circuit of claim 66, wherein

the radio frequency integrated circuit is a transceiver and further includes,

an input receiver to receive a serial digital transmission bit stream from the another integrated circuit;

a data recoverer coupled to the input receiver, the data recoverer to recover digital data bits from the serial digital transmission bit stream;

a low pass filter coupled to the data recoverer, the low pass filter to convert the digital data bits into an analog transmission signal;

a mixer coupled to the low pass filter, the mixer to up-convert the analog transmission signal from a baseband frequency to a second selectable carrier frequency as a transmit radio frequency signal; and

an amplifier coupled to the mixer, the amplifier to amplify the transmit radio frequency signal for broadcast over the antenna.

70. The radio frequency integrated circuit of claim 69, wherein,

the serial digital transmission bit stream has a reduced output voltage swing to further reduce noise, and

the input receiver to increase the output voltage swing of the serial digital transmission bit stream in the radio frequency integrated circuit.

71. A system comprising:

a radio frequency integrated circuit including

a single bit sigma delta modulator with an analog input and a serial digital output, and

an output driver having an input coupled to the serial digital output of the single bit sigma delta modulator, the output driver having a differential output;

and

a digital signal processing integrated circuit including

an input receiver coupled to the output driver of the radio frequency integrated circuit, the input receiver having a differential input to couple to the differential output of the output driver, the input receiver having a serial digital output.

72. The system of claim 71, wherein

the output driver to drive a serial digital bit stream out from the radio frequency integrated circuit with a low voltage differential output swing to lower noise.

73. The system of claim 72, wherein

the input receiver to receive the serial digital bit stream with the low voltage differential output swing.

74. The system of claim 71, wherein

the digital signal processing integrated circuit further includes

a decimator coupled to the serial digital output of the input receiver, the decimator having a parallel digital output, and

a demodulator coupled to the parallel digital output of the decimator.

75. A radio frequency integrated circuit comprising:

a gain amplifier having an input to couple to an antenna, the gain amplifier having an analog output;

a down converter having an analog input coupled to the analog output of the gain amplifier, the down converter having an analog output;

a single bit sigma delta modulator having an analog input coupled to the analog output of the down converter, the single bit sigma delta modulator having a serial digital output; and

an output driver having an input coupled to the serial digital output of the single bit sigma delta modulator, the output driver having a differential output.

76. The radio frequency integrated circuit of claim 75, wherein

the radio frequency integrated circuit is a radio frequency receiver integrated circuit.

77. The radio frequency integrated circuit of claim 75, wherein

the radio frequency integrated circuit is a transceiver and further includes,

an input receiver having a differential input, the input receiver having a serial digital output;

a data recoverer having an input coupled to the serial digital output of the input receiver, the data recoverer having a serial digital output;

a low pass filter having an input coupled to the serial digital output of the data recoverer, the low pass filter having an analog output;

a mixer having an input coupled to the analog output of the low pass filter, the mixer having an analog output; and

an amplifier having an input coupled to analog output of the mixer, the amplifier having an output to couple to the antenna.

78. A system comprising:

a radio frequency integrated circuit including

a modulating analog to digital converter with a single bit output, the modulating analog to digital converter to convert an analog input signal into a serial digital bit output stream, and

an output driver coupled to the single bit analog to digital converter, the output driver to drive the serial digital bit stream out from the radio frequency integrated circuit;

and

a processor coupled to the radio frequency integrated circuit.

79. The system of claim 78, wherein

the processor includes

an input receiver coupled to the output driver of the radio frequency integrated circuit, the input receiver to receive the serial digital bit stream.

80. The system of claim 79, wherein the processor is a digital signal processor and further includes

a decimator coupled to the input receiver, the decimator to receive the serial digital bit stream, lower a sampling rate of the serial digital bit stream, and convert the serial digital bit stream into parallel digital data samples, and

a demodulator to digitally demodulate the parallel digital data samples into data words for further signal processing by the digital signal processing integrated circuit.

81. The system of claim 79, wherein the processor includes programmable instructions to provide

a decimator coupled to the input receiver, the decimator to receive the serial digital bit stream, lower a sampling rate of the serial digital bit stream, and convert the serial digital bit stream into parallel digital data samples; and

a demodulator coupled to the decimator, the demodulator to digitally demodulate the parallel digital data samples into data words for further signal processing by the digital signal processing integrated circuit.

82. A system comprising:
a radio frequency integrated circuit including
a modulating analog to digital converter with an analog input and a serial digital output, and
an output driver having an input coupled to the serial digital output of the modulating analog to digital converter, the output driver having a digital output;
and
a processor coupled to the radio frequency integrated circuit.

83. The system of claim 82, wherein
the processor includes
an input receiver coupled to the digital output of the output driver of the radio frequency integrated circuit, the input receiver having a digital input to couple to the digital output of the output driver, the input receiver having a serial digital output.

84. The system of claim 83, wherein
the processor is a digital signal processor and further includes
a decimator coupled to the serial digital output of the input receiver, the decimator having a digital output, and
a demodulator coupled to the digital output of the decimator.

85. The system of claim 83, wherein

the processor includes programmable instructions to provide

a decimator coupled to the serial digital output of the input receiver, the decimator having a digital output, and

a demodulator coupled to the digital output of the decimator.